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# ON ONE SCHEME OF MULTICHANNEL ARBITRE

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# ԲԱԶՄԱԿԱՆԱԼ ԱՐԲԻՏՐԻ ՄԻ ՍԽԵՄԻ ՄԱՍԻՆ

Նկարագրված է բազմականալ արբիտրի պարզ սխեմ, որը բացառում է ընդունիչի մուտքում ընդհարումները այն դեպքում, երբ դեպի նա են ուղղվում մի քանի անկախ աշխատող սարքավորումներ:

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# ON ONE SCHEME OF MULTICHANNEL ARBITRE

A simple scheme of multichannel arbitre is described, which excludes collisions on the receiver input when the latter is accessed to by some independently running devices.

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А.Р.МАТЕВОСЯН

# ОБ ОДНОЙ СХЕМЕ МНОГОКАНАЛЬНОГО АРБИТРА

Описана простая схема многоканального арбитра, исключающего конфликты на входе приемника при обращении к нему нескольких независимо работающих устройств.

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In solving some practical problems in networking of interaction between a few independently running devices (sources) with one and the same receiver (specifically, in designing the multiprocessor systems with common resources), one encounters the problem of removing the collisions on the receiver input. In this case solution is attained by using various arbitres [1]. The existing schemes of arbitres are rather complicated. Thus, in [2] the equipment for interfacing two microcomputers with common memory is described whose arbitre scheme contains by two NO and AND elements as well as an RS-flip-flop. This arbitre has 2 inputs and 2 outputs, providing connection of one of the microcomputers to the common memory, interdicting at the same time the access of the second one to the same memory cells. In increasing the number of inputs the arbitres schemes become even more complicated [3] .

This paper is devoted to the description of a new, to our mind original arbitre which differs from the well-known ones by maximum simplicity.

The mode of operation of the suggested arbitre is based on the RS-flip-flop connection in indeterminate behaviour [4] .

The functional scheme of the RS-flip-flop connection on the OR-NO elements as a two-channel arbitre for controlling the access of two sources $S_1$ and $S_2$ to the receiver R is shown in Fig.1.

In the initial state signals in logic-1 level come from the sources $S_1$ and $S_2$ on the RS-flip-flop inputs (elements $D_1$ and $D_2$) (see the time diagram in Fig.2). Hence, flip-flop's Q and $\bar{Q}$ outputs have logic-0 levels, which interdicts information transmission from both sources to the receiver and back. Let now the source $S_1$ requests work with the receiver (on flip-flop's R-input the signal level becomes equal to logic-0). Then, on the flip-flop Q-output the level-1 is set, which allows the information transmission from the first source to the receiver (through elements $D_4$ and $D_7$) as well as the answer of the receiver to this source (through element $D_3$). This state of the RS-flip-flop retains all the time, until there is logic-0 level on its R-input irrespective of the signal's level changes on the S-input. On finishing the first source's work level-1 is recovering on flip-flop's R input. If at this time there was also level-1 on flip-flop's input, the flip-flop would return to its initial state. But if at this time the second source requested work with the receiver (on S-input there was "0"), then flip-flop's state would change to the opposite, and on $\bar{Q}$-output "1" will be set. Thereby, the information transmitting channels will open from the second source to the receiver (through elements $D_5$ and $D_7$) and back (through element $D_6$). This state of the flip-flop will retain during all the work-time of the second source with the receiver irrespective



of the changes in signal's level on R-input (irrespective of the requests of the first source). On finishing the second source work and lifting the level "0" on S-input the flip-flop's state is defined by the signal's level on R-input by analogy with described above.

If both sources simultaneously request work with the receiver (simultaneously move "0" levels on flip-flop's inputs), then on one flip-flop's output "1" will be set in, and on the other "0" will remain. And besides, level "1" will be set in precisely on that of elements $D_1$ and $D_2$ output which has the least delay of signal's passage from input to output (in view of inabsolute identity of these elements because of technological spread of parameters in manufacturing). Proceeding from the condition of sources independence, no supernumerary situations will appear in that case, as long as the receiver will work with only one of them in any case. To signal the sources about the receiver's availability, the signals from flip-flop's output may be put into the corresponding sources (see Fig.1, dotted), or we may judge about it analyzing the coming ACK-signal (off-hook signal from the receiver).

All afore-said is correct also in the case when RS-flip-flop is realized on AND-NO elements, but in this case the levels of all mentioned signals will be changed to the contrary. Such realization of RS-flip-flop may be used, for example, to control the joining of analogous signals through the analogy switches K590 KH2.

Thus, RS-flip-flop's ability to work in indeterminate mode provides the possibility to control the work of two independent

sources with one receiver without any collisions, and in this case the priority of the first requested source is ensured for all the time of its work with the receiver. Obviously, the RS-flip-flop's work as a two-channel arbitre doesn't depend on selecting the base of elements.

In practice often more than 2 sources are used. In that case the described effect on the example of RS-flip-flop may be applied to any number of sources. So, in Fig.3 the functional scheme of connection of four-channel arbitre is presented which provides control of switching four independently running sources $S_1$-$S_4$ to one receiver R. At initial time moment from all the sources to the input request of the corresponding elements OR-NO the logic-1 level signals come, i.e. none of the sources request work with the receiver. Then the receiver is switched off from all the sources. As soon as one of the sources requests work with the receiver (it will set "0" on input of the corresponding OR-NO element), on the corresponding OR-NO elements output "1" will be set and information transmitting channels will be opened from that source to the receiver. Simultaneously level "1" from this OR-NO element output will come to all other OR-NO elements inputs, which will not allow the other sources to work with the receiver, even in the presence of requests from them. This state of arbitre will retain for all the work-time of the first requested source with the receiver. The release of the receiver from this source is realized by setting "1" on OR-NO element's request-input. The arbitre's state is defined with request inputs status of the rest of the sources: if there are not requests,



the arbitre will return to its initial state, but if there are requests, then on only one of the OR-NO elements output "1" will be set (namely of the one whose delay of signal's passage from input to output is analogous to the RS-flip-flops because the technological spread is most minimal). The same state of arbitre will be set in the case of simultaneous receiving of requests from several sources in the initial state.

Thus, in ongoing moment level "1" may be on only one of the arbitre's outputs even in the presence of several requests, and on the rest of its outputs "0" levels will be, i.e. in every instant only one source can work with the receiver. The above-described four-channel arbitre is put in the scheme of controlling the switching of four computers of different types to one printer.

It's obvious that increasing the number of OR-NO elements and their inputs it is possible to obtain the arbitre for controlling any number of channels.

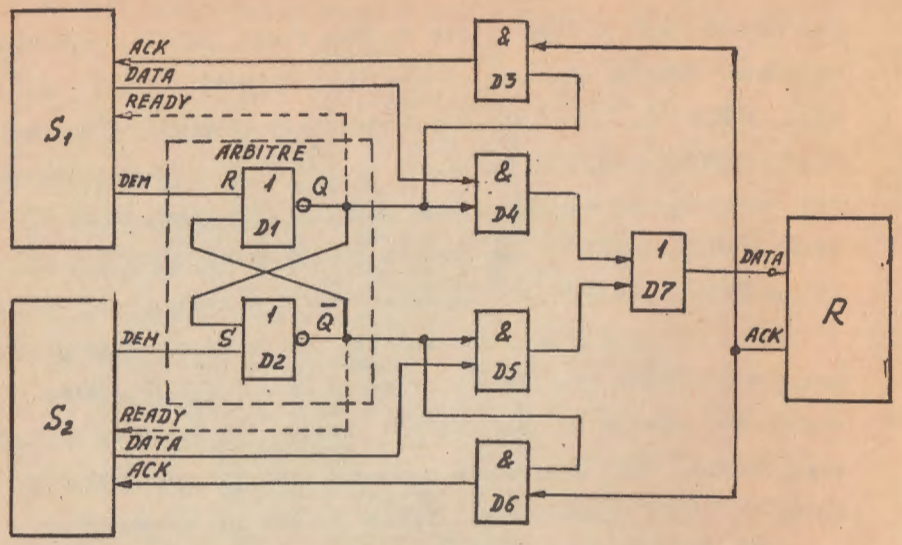


Fig.1

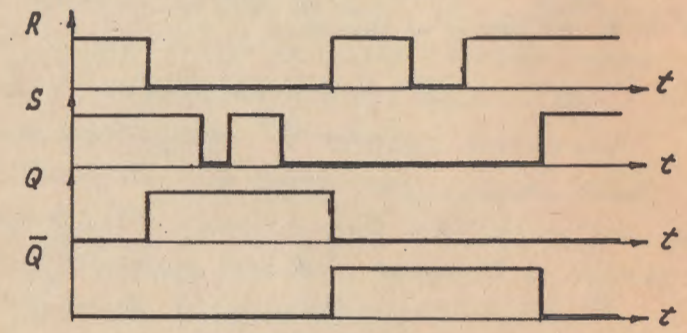


Fig.2.



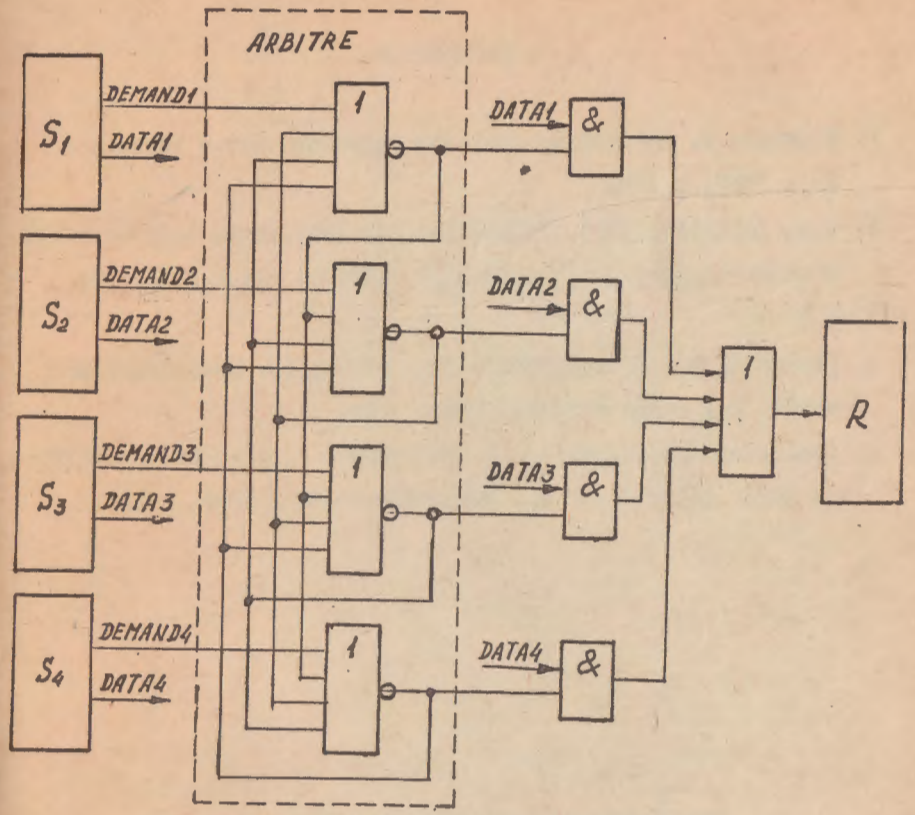


Fig.3

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